

ABSTRACT

There is provided a semiconductor memory device capable of eliminating the occurrence of delays in access when switching from a standby state to an active state. A drain voltage generator 10A generates a predetermined drain voltage MCD which is low in driving performance owing to PMOS15, 17 and NMOS16, 18 each having large ON resistance irrespective of the presence of a chip selection signal and apply the drain voltage to each of memory arrays. When read operation is started when a chip selection signal /CE goes "L", the drain voltage MCD is generated by PMOSs 11, 15 and NMOSs 12 to 14 with a predetermined driving performance. As a result, a predetermined drain voltage MCD is always applied when switching from a standby state to an active state, thereby eliminating the occurrence of delays in access to a memory cell.